PVP 14

Code: EE2T4

I B.Tech - II Semester – Regular Examinations – April 2016

BASIC ELECTRONIC DEVICES AND CIRCUITS
(ELECTRICAL & ELECTRONICS ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) Differentiate between static and dynamic resistances.
   b) Explain diode as a switch.
   c) Give any four advantages of FET over BJT.
   d) Differentiate between enhancement mode and depletion mode operations of MOSFET.
   e) Define stability factors S, $S^{|}$ and $S^{||}$.
   f) Explain need for biasing.
   g) Draw the transistor hybrid model circuit.
   h) Write the Barkhausen criterion.
   i) What are the advantages of negative feedback?
   j) Write the applications of RC oscillators.
   k) Why CC amplifier called as Emitter follower?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks. 3 x 16 = 48 M

2. a) Draw I-V characteristics of a silicon junction diode and explain. 8 M

b) Derive the expression for ripple factor of full wave rectifier with capacitor filter. 8 M

3. a) A BJT has α=0.99, I_B=25μA and I_{CBO}=200nA. Find
i) the dc collector current
ii) the dc emitter current and
iii) the percentage error in emitter current when leakage current is neglected. 8 M

b) Explain the operation of JFET with neat drain characteristics. 8 M

4. a) Explain the different bias compensation techniques to reduce the drift of the operating point. 8 M

b) Explain the self bias circuit and derive the operating point. 8 M

5. a) Analyze a Single stage transistor amplifier using h-parameters. 8 M

b) Derive the high frequency parameters transconductance and input conductance of a transistor in terms of low frequency parameters. 8 M

6. a) Draw and explain the RC phase shift oscillator. Also derive the condition for oscillations. 8 M

b) Draw and explain feedback topologies. Give the effect of negative feedback on input and output resistances of these topologies. 8 M